AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 3 and 13 without prejudice.

1. (CURRENTLY AMENDED) An apparatus comprising:

a memory comprising a first address space configured as read only and a second address space configured as read and write, wherein said memory returns a first data item in response to a first address within said first address space;

a logic circuit configured to (i) deassert a command signal in response to said first address not matching any of a plurality of predetermined addresses and (ii) generate a first branch instruction and assert said command signal in response to said first address matching one of said predetermined addresses in response to said matching, wherein said logic circuit is further configured to generate a first branch address within said second address space and assert said command signal in response to a second address (i) immediately following said first address and (ii) having a value one unit of said first address space different than said first address; and

a multiplexer configured to select (i) said first data item from said memory or (ii) said first branch instruction from said logic circuit in response to said command signal.

2. (ORIGINAL) The apparatus according to claim 1, wherein said memory comprises a read only memory (ROM) and a random access memory (RAM).

3. (CANCELED)

4. (CURRENTLY AMENDED) The apparatus according to claim 1 ~~3~~, further comprising:

a processor having (i) an address bus directly connected to said memory and said logic circuit and (ii) a data bus directly connected to said multiplexer.

5. (CURRENTLY AMENDED) The apparatus according to claim 1 ~~3~~, wherein said logic circuit comprises:

a first section configured to generate a plurality of match signals by comparing said first address to each of said predetermined addresses.

6. (ORIGINAL) The apparatus according to claim 5, wherein said logic circuit further comprises:

a second section configured to generate an indication signal in response to (i) said match signals and (ii) a difference between said first address and said second address.

7. (ORIGINAL) The apparatus according to claim 6, wherein said logic circuit further comprises:

a third section configured to generate said command signal in response to said indication signal and said match signals.

8. (CURRENTLY AMENDED) The apparatus according to claim 1 ~~3~~, wherein said logic circuit comprises:

an adder configured to generate an intermediate address by adding said one unit to said first address.

9. (ORIGINAL) The apparatus according to claim 8, wherein said logic circuit further comprises:

a comparator configured to compare said intermediate address with said second address.

10. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said memory is writeable in said second address space for storing (i) a second branch instruction and (ii) a second branch address within said first address space ~~range~~.

11. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said first address space is configured to address ~~addresses~~ read only memory cells and said second address space is configured to address ~~addresses~~ read and write memory cells.

12. (CURRENTLY AMENDED) A method for reading from a memory space comprising a first address range and a second address range, comprising the steps of:

(A) returning a first data item in response to a first address within said first address range;

(B) generating a first branch instruction in response to said first address matching one of said predetermined addresses;

(C) selecting said first data item in response to said first address not matching any of said predetermined addresses; ~~and~~

(D) selecting said first branch instruction in response to step (B); and

(E) returning a first branch address within said second address range in response to a second address (i) immediately following said first address and (ii) having a value one unit of said first address range different than said first address.

13. (CANCELED)

14. (ORIGINAL) The method according to claim 12, further comprising the step of:

returning a second data item stored in said second address range in response to receiving said first branch address.

15. (ORIGINAL) The method according to claim 14, further comprising the step of:

returning a second branch instruction stored in said second address range in response to receiving a third address after said first branch address.

16. (ORIGINAL) The method according to claim 15, further comprising the step of:

returning a second branch address (i) within said first address range and (ii) stored in said second address range at a fourth address received after said third address.

17. (ORIGINAL) The method according to claim 12, further comprising the step of:

branching a first program stored in said first address range to a second program stored in said second address range in response to said first branch instruction and said first branch address.

18. (ORIGINAL) The method according to claim 12, further comprising the step of:

ignoring said first branch instruction while executing a first program stored in said first address range.

19. (ORIGINAL) The method according to claim 12, wherein said first address range comprises read only and said second address range comprises read and write.

20. (CURRENTLY AMENDED) An apparatus for reading from a memory space comprising a first address range and a second address range, comprising:

means for returning a first data item in response to a first address within said first address range;

means for generating a first branch instruction in response to said first address matching one of said predetermined addresses;

means for generating a first branch address within a second address range and asserting a command signal in response to a second address (i) immediately following said first address and (ii) having a value one unit of said first address range different than said first address;

means for selecting said first data item in response to said first address not matching any of said predetermined addresses; and

means for selecting said first branch instruction in response to said means for generating said first branch instruction.

21. (NEW) An apparatus comprising:

a memory comprising a first address space configured as read only and a second address space configured as read and write, wherein said memory returns a first data item in response to a first address within said first address space;

a logic circuit configured to (i) deassert a command signal in response to said first address not matching any of a plurality of predetermined addresses and (ii) generate a first branch instruction and assert said command signal in response to said first address matching one of said predetermined addresses in response to said matching, wherein said logic circuit includes a comparator configured to generate said command signal by comparing (i) an intermediate address generated by adding one to said first address with (ii) a second address immediately following said first address; and

a multiplexer configured to select (i) said first data item from said memory or (ii) said first branch instruction from said logic circuit in response to said command signal.